Amendments to the Drawings:

New corrected drawings in compliance with 37 CFR 1.121(d) have been included as per Examiner request. Please replace FIGS. 1-7 with amended FIGS. 1-7.

Attachment: Replacement Sheets

Remarks/Arguments

In the Office Action mailed 12/21/2004, Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Murphy (Murphy), U.S. patent no.5,128,970.

Applicant respectfully submits that a prima facie case of obviousness with respect to the pending claims has not been established. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). MPEP §2143.

Examiner admits that the AAPA does not explicitly disclose that first clock domain gating circuit being configured to toggle a state of a signal on said first output terminal from one of a first state and a second state to the other of said first state and said second state every time a pulse is detected in said input signal, thereby producing a latched output at said first output terminal. In addition, AAPA does not explicitly disclose that second clock domain gating circuit being configured to produce a pulse on said output signal at said second output terminal, said pulse on said output signal having a duration at least as long as a period of said second clock every time a state of said latched output changes.

Murphy discloses that a logic circuit to perform said first clock domain gating circuit being configured to toggle a state of a signal on said first output terminal from one of a first state and a second state to the other of said first state and said second state every time a pulse is detected in said input signal, thereby producing a latched output at said first output terminal. Murphy also discloses that another logic circuit to perform said second clock domain gating circuit being configured to produce a pulse on said output signal at said second output terminal, said pulse on said output signal

having a duration at least as long as a period of said second clock every time a state of said latched output changes.

However, as described in the Abstract, Murphy is specifically directed toward creating a output signal that is synchronized to a system clock signal, from an asynchronous input strobe signal which can occur at any point in a given clock cycle. That is, only a single signal is synchronized.

In contrast, the present invention is directed toward an integrated circuit configured to capture an input signal to produce an output signal. The input signal is synchronized with a first clock signal. The output signal is synchronized with a second clock signal having a second frequency different from a first frequency associated with the first signal. That is, both signals are synchronized. Hence, there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.

In view of the discussion herein, Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner.

Additionally, the Commissioner is authorized to charge any fees beyond the amount enclosed which may be required, or to credit any overpayment, to Deposit Account No. 50-2284 (Order No. ATEC-P005/SNG-024A).

Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at 408-257-5500.

Respectfully submitted,

/Alex Sousa/

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